SiliconMotion

WHITE PAPER

Silicon Motion's FerriSSD®

For Embedded Boot Load Applications

Introduction

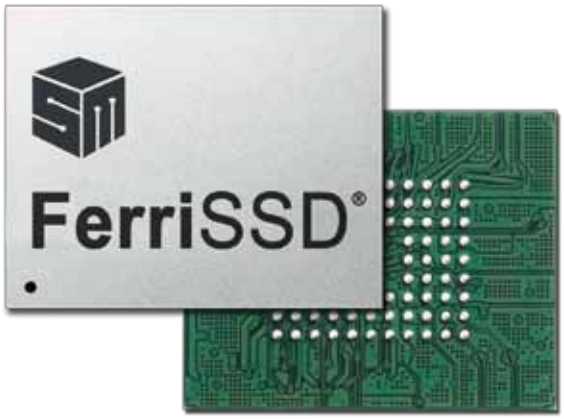
Silicon Motion's FerriSSD® Product Family was developed to satisfy the unique and demanding requirements of boot loaders in embedded applications. Embedded boot load SSDs are distinguished by low - to medium-density, coupled with a high data integrity requirement, in various operating temperature environments. SSD boot loaders have a very low tolerance for data faults, since boot load SSDs must load and run OS and/or software without interruption or error. In comparison, mass market SSDs are typically designed for cost-sensitive consumer sectors, such as consumer entertainment audio/video applications, which might tolerate some data errors.

In order to meet uncompromising boot load SSD performance specifications, SMI's FerriSSD Family currently incorporates four unique technologies that enhance the data integrity, longevity and price / performance of SSD boot loaders:

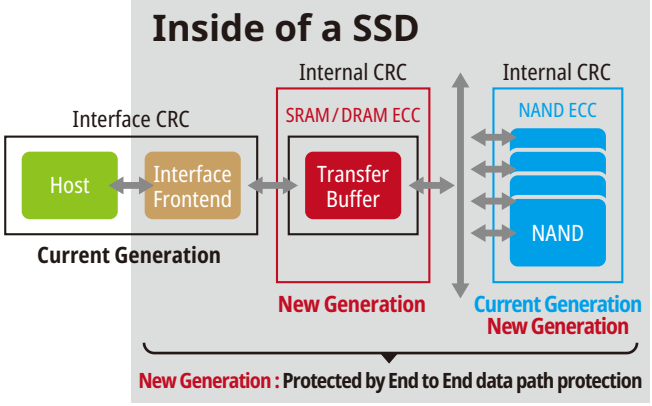
- End-to-end Data Path Protection
- NANDXtend™
- IntelligentScan & DataRefresh
- Hybrid Zone

End-to-end Data Path Protection: no data errors will be sent to host

Conventional SSDs may employ error detection and correction circuitry at the far ends of the data path: at the front-end host interface and at the back-end

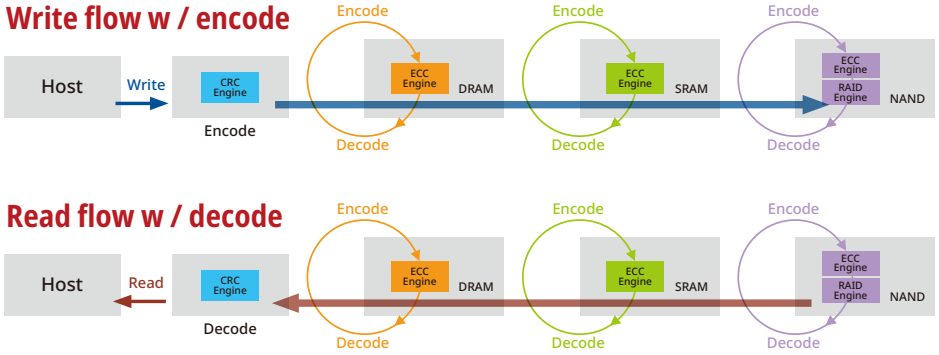


NAND interface. This omits an important gap at the internal SRAM and/or DRAM transfer buffers, and other circuit paths. Data errors that occur between the NAND interface and the host, such as soft error bits, are often difficult to identify and duplicate. While conventional SSDs may have some internal error detection circuitry, SMI's FerriSSDs incorporate full data recovery engines to provide enhanced data integrity throughout the entire Host-to-NAND-to-Host data path.



The FerriSSD data recovery algorithm can effectively detect any error in the SSD data path, including hardware (i.e. ASIC) errors, firmware errors and memory errors arising in SRAM, DRAM or NAND. The latest generation FerriSSD implements redundant backup--SMI Ferri Group Page Raid--which further eliminate the possibility of uncorrectable error.

Should FerriSSD identify any error that cannot be corrected, it will pass an error flag to the host for appropriate recovery processing. By comparison, conventional SSDs pass faulty data to the host without an error flag, exacerbating the initial problem by failing to alert the host to the need for error recovery processing.

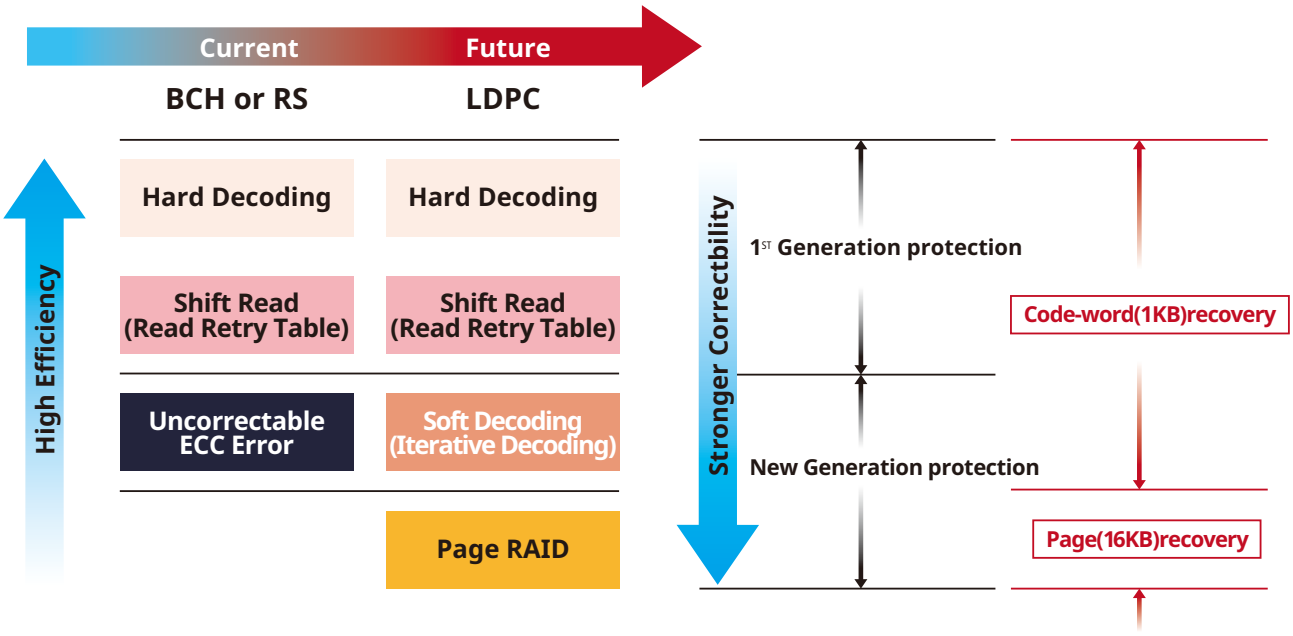


- Whole SSD error Detection
- DRAM error Detection with Correction
- SRAM error Detection with Correction
- NAND Flash ECC Detection with Correction
  - > Hard-decode (BCH)
  - > Soft-decode (LDPC)
  - > Group page RAID

No error data will be sent to host!

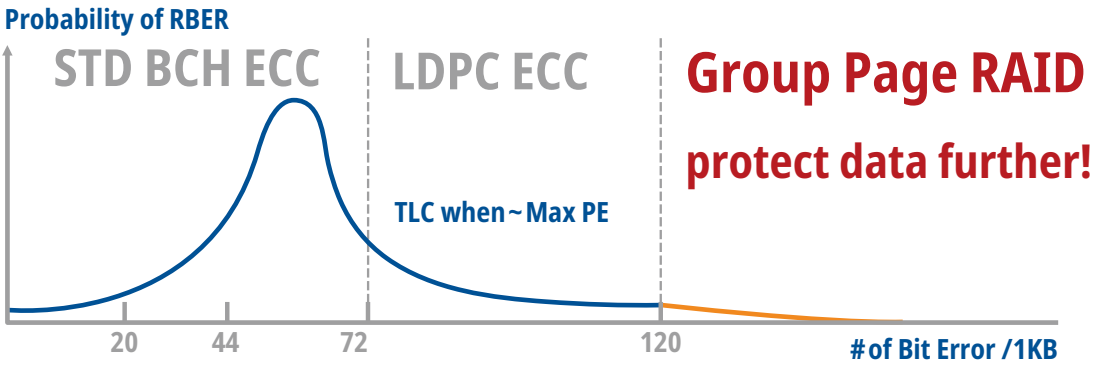
NANDXtend :
extend the life of SSD with lower dPPM

Conventional SSDs employ BCH and RS ECC (error correction code) engines to detect errors and initiate first-level correction using NAND shift-read-retries. In addition to this first-level error correction, FerriSSDs also implement a highly efficient second-level correction scheme using an LDPC (low-density parity check) code and a Group page RAID algorithm (a highly efficient redundant backup). The combination of Ferri Group page RAID and SMI's 4th generation LDPC ECC engine, results in uncompromised data integrity, while delivering faster throughput compared to competing implementations.



After accumulated use (i.e. P/E) cycles, NAND memory cells will begin to deteriorate, increasing both the probability and the magnitude of raw error bits. SMI's advanced Group page RAID algorithm, implemented by Ferri NANDXtend, corrects for larger 16KB code-word unit errors, providing a critical second-level of protection compared to 1KB code-word unit ECC engines used in conventional SSDs.

The specific Group Page RAID algorithm implemented by SMI NANDXtend is uniquely suited for low- and medium-density SSD drives typical used in boot load applications. This not only extends SSD life expectancy, but also significantly reduces lifetime dPPM.



IntelligentScan & DataRefresh :
proactive data loss prevention measures

To prevent potential data loss, FerriSSD "IntelligentScan" proactively scans and refreshes (DataRefresh) NAND memory to enhance data integrity by taking precautionary steps before errors might occur. This becomes increasingly important as the aggregate number of P/E cycles accumulate.

Thermo impact on NAND Data Retention

Temp	SLC @ max PE	MLC @ max PE
40	75.58 Mo	12 Mo
55	12 Mo	1.88 Mo
70	2.14 Mo	0.34 Mo
85	0.45 Mo	0.07 Mo

Thermal Impact on Data Retention

One of the most significant inhibitors to data retention is elevated NAND temperature. FerriSSDs incorporate a patent-pending monitoring algorithm that logs cumulative junction temperature readings, the number of P/E cycles, SSD power on-time, and other essential reference points to dynamically select and prioritize which NAND cells to DataRefresh, and when. IntelligentScan & DataRefresh work together to significantly extend the retention capability before data becomes unrecoverable.

Read Disturbance

Excessive read cycles from a specific cell can also lead to un-intended over-charging of adjacent cells, leading to unrecoverable bit errors. FerriSSDs avoid potential read disturbance errors through periodic IntelligentScan & DataRefresh of NAND blocks that undergo repetitive read cycles.

The FerriSSD firmware--an advanced 4th generation algorithm (IntelligentScan)-- automatically manages DataRefresh cycles and processing time to minimize data loss due to both thermal impacts and read disturbances.

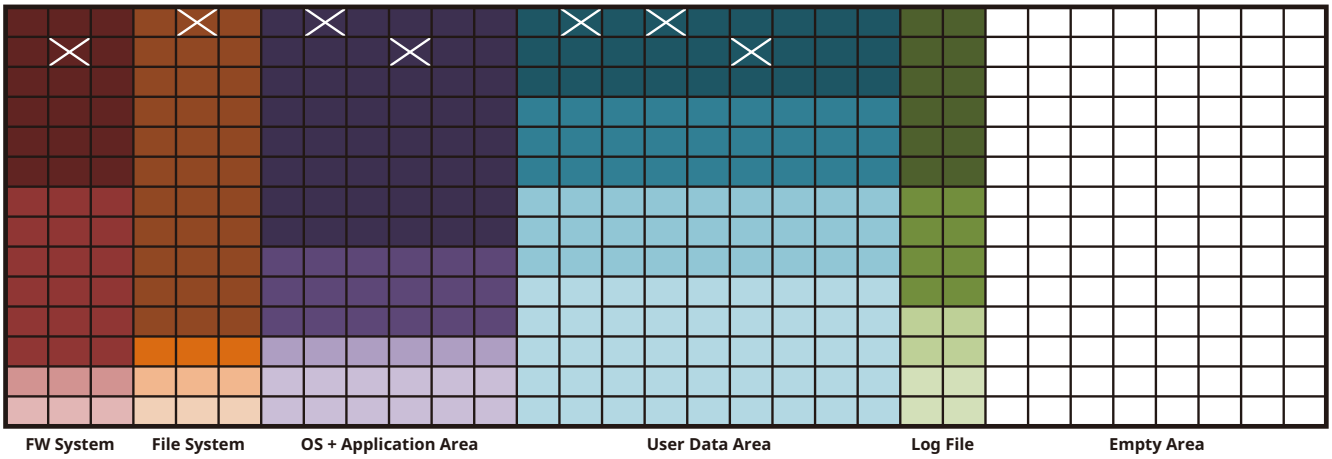
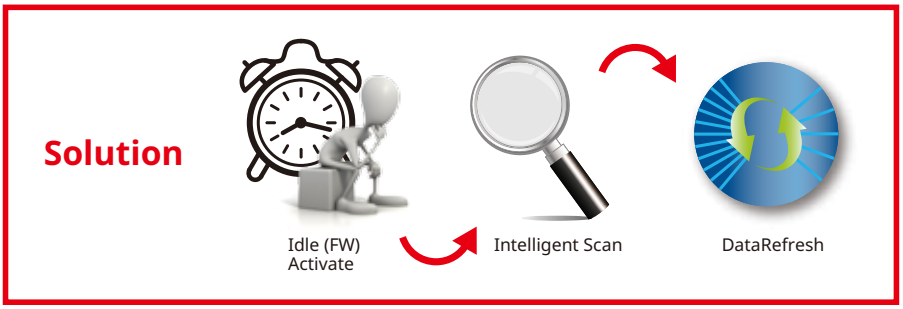


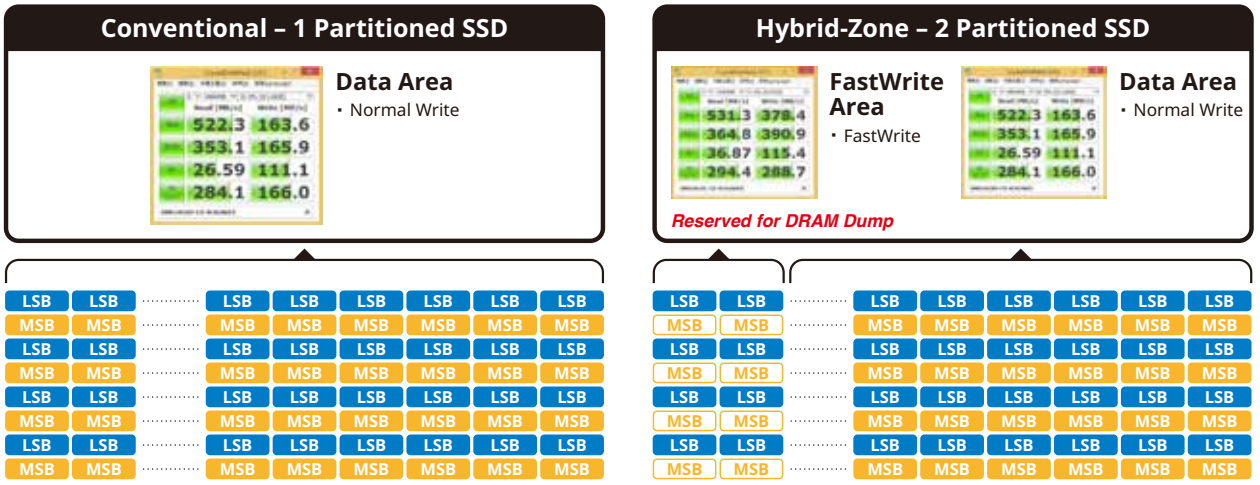
Illustration	Description
	= access extremely frequently
	= access hourly/daily
	= access weekly
	= access montly
	= access yearly or less



Hybrid Zone :
ideal blend of cost, reliability and performance

Conventional SSDs configure on-board NAND die as single-layer cells (SLC), multi-layer cells (MLC), or the new 3D triple-layer cells (TLC). The selection of SLC vs. MLC vs. TLC is based on the memory density vs. access latency trade-off inherent in each cell type. FerriSSDs offer a Hybrid Zone, the unique capability of partitioning a single NAND die into separate SLC and MLC/TLC zones.

The Hybrid Zone feature--enabling the partition of a single drive--is particularly useful in low- to medium-density SSDs. Without foregoing the density benefits of MLC/TLC, single NAND die SSDs can still maintain fast write SLC memory, which is ideal for emergency power shutdown operation. Without a portion of memory implemented as SLC, both the cost and the size of battery storage needed for MLC/TLC power shutdown would increase. The implementation of SLC memory is ideal for high reliability and fast access--assigning SLC to boot code for instance-- while also preserving a portion of the NAND die for higher density MLC/TLC uses.



Conclusion

Boot load SSDs targeted at embedded applications embody a number if unique requirements. In addition to the ever-present need for minimal cost, boot load SSDs must maintain an especially high level of data integrity, even as they operate in often remote and inhospitable environments. SMI engineers have developed a number of advanced technologies that enhance the life, data integrity and cost / performance of its FerriSSD family, which now incorporates a proven 4th generation algorithm.

For more information about Ferri Family, please go to **www.siliconmotion.com** or send email to **ferri@siliconmotion.com**